AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1 to 22 (Cancelled)

23. (New) A method, comprising:

sending a query from a graphical user interface to a hardware configuration database, the query requesting, information located within a simulation model, the hardware configuration database including locations of hardware devices, the hardware devices representing functional processes;

searching the functional processes to locate the information; and

directly accessing the information in the simulation model from the graphical user interface without assistance from the hardware configuration database.

24. (New) The method of claim 23, wherein the functional processes represent a chip design.

25. (New) The method of claim 24, wherein the chip design represents a processor chip.

26. (New) The method of claim 23, further comprising combining the functional processes into a first level of hierarchical relationships.

27. (New) The method of claim 26, further comprising combining the first level hierarchical relationships into a second level of hierarchical relationships.

28. (New) The method of claim 27, further comprising repeatedly combining the hierarchical relationships until a chip design is described.

29. (New) The method of claim 23, wherein the simulation model is a first simulation model and further comprising changing the hardware descriptions stored in the database to forma second simulation model.

30. (New) The method of claim 23, wherein the query includes requests for information on a processor chip design.

31. (New) An apparatus comprising:

circuitry to:

send a query from a graphical user interface to a hardware configuration database, the query requesting, information located within a simulation model, the hardware

configuration database including locations of hardware devices, the hardware devices representing functional processes;

search the functional processes to locate the information; and

directly access the information in the simulation model from the graphical user interface without assistance from the hardware configuration database.

32. (New) The apparatus of claim 31, wherein the functional processes represent a chip design.

33. (New) The apparatus of claim 32, wherein the chip design represents a processor chip.

34. (New) The apparatus of claim 31, further comprising circuitry to combine the functional processes into a first level of hierarchical relationships.

35. (New) The apparatus of claim 34, further comprising circuitry to combine the first level hierarchical relationships into a second level of hierarchical relationships.

36. (New) The apparatus of claim 35, further comprising circuitry to combining repeatedly the hierarchical relationships until a chip design is described.

37. (New) The repeatedly of claim 31, wherein the simulation model is a first simulation model and further comprising circuitry to change the hardware descriptions stored in the database to form a second simulation model.

38. (New) The method of claim 31, wherein the query includes requests for information on a processor chip design.

39. (New) An article comprising a machine-readable medium that stores executable instructions causing a machine to:

send a query from a graphical user interface to a hardware configuration database, the query requesting, information located within a simulation model, the hardware configuration database including locations of hardware devices, the hardware devices representing functional processes;

search the functional processes to locate the information; and

directly access the information in the simulation model from the graphical user interface without assistance from the hardware configuration database.

40. (New) The article of claim 39, wherein the functional processes represent a chip design.

41. (New) The article of claim 40, wherein the chip design represents a processor chip.

42. (New) The article of claim 39, wherein the medium further comprises instruction causing a machine to combine the functional processes into a first level of hierarchical relationships.

43. (New) The apparatus of claim 42, wherein the medium further comprises instruction causing a machine to combine the first level hierarchical relationships into a second level of hierarchical relationships.

44. (New) The apparatus of claim 43, wherein the medium further comprises instruction causing a machine to combine repeatedly the hierarchical relationships until a chip design is described.

45. (New) The repeatedly of claim 39, wherein the simulation model is a first simulation model and the medium further comprises instruction causing a machine to change the hardware descriptions stored in the database to form a second simulation model.

46. (New) The method of claim 39, wherein the query includes requests for information on a processor chip design.